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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,273	05/17/2005	Yusuke Otomo	6700-85366	3734

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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
08/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,273	OTOMO ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *2-4,7,8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 10* is/are allowed.

6)☒ Claim(s) *3,4,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5/17/05, 2/26/07.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/3/2007 has been entered.

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Holmqvist (US 5220275).

With respect to claim 3, Figure 3 of Holmqvist discloses a phase comparator circuit (31, 32, 33, 34, 35 and 36) for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal (Input signal), said phase comparator circuit characterized in that; a first phase error signal, representing the phase difference between the transition point of said data signal (Input signal), and the rising edge of a first clock signal as the pulse width, is outputted, wherein the pulse width of said first phase error signal is extended by the time width corresponding to the unit time width of said data signal; and a second phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a second clock signal as being the inverted clock signal of said first clock signal, is outputted, wherein the pulse width of said second phase error signal is extended by the time width corresponding to the unit time width of said data signal.

With respect to claim 4, Figure 3 of Holmqvist discloses the phase comparator circuit (31, 32, 33, 34, 35 and 36) as defined in claim 3, wherein, when the transition has occurred between 2 consecutive data in said data signal (input signal), a first reference signal (clock state), having a time width ranging from the rising edge of said second clock signal to the rising edge of said first clock signal, is outputted in order to determine the increase or the decrease of the pulse width of said first phase error signal; and when the transition has occurred between 2 consecutive data in said data signal, a second reference signal, having a time width ranging from the rising edge of said first clock signal to the rising edge of said second clock signal (fire signal), is outputted in order to determine the increase or decrease of the pulse width of said second phase

error signal.

5. Claims 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Summers (GB 2089601).

With respect to claim 3, Figure 7 of Summers discloses a phase comparator circuit (701-706 and 710) for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal (DP), said phase comparator circuit characterized in that; a first phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a first clock signal as the pulse width, is outputted; wherein the pulse width of said first phase error signal is extended by the time width corresponding to the unit time width of said data signal; and a second phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a second clock signal as being the inverted clock signal of said first clock signal, is outputted.

With respect to claim 4, Figures 7 and 9 of Summers discloses a phase comparator circuit as defined in claim 3, wherein, when the transition has occurred between 2 consecutive data in said data signal (DP), a first reference signal (905), having a time width ranging from the rising edge of said second clock signal to the rising edge of said first clock signal (CK), is outputted in order to determine the increase or the decrease of the pulse width of said first phase error signal; and when the transition has occurred between 2 consecutive data in said data signal, a second reference signal (906), having

a time width ranging from the rising edge of said first clock signal to the rising edge of said second clock signal, is outputted in order to determine the increase or decrease of the pulse width of said second phase error signal, wherein the pulse width of said second phase error signal is extended by the time width corresponding to the unit time width of said data signal.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US 5359298) in further view of Summers (GB 2089601 A).

With respect to claim 7, Figure 1 of Abe discloses a CDR circuit including a phase comparator circuit (12 and 22), a charge pump circuit (14 and 24) and a loop filter (16 and 26), operating with a clock signal (CLK) whose period is 2 times the unit time width of an inputted data signal, and characterized in that; said phase comparator circuit outputs a first phase error signal, representing the pulse width as being the phase difference between the transition point of the said data signal and the rising edge of said clock signal, the pulse width of said first phase error signal being extended by the time

width corresponding to the unit time width of said data signal and a second phase error signal, representing the pulse width as being the phase difference between the transition point of said data signal and the falling edge of said clock signal, the pulse width of said second phase error signal being extended by the time width corresponding to the unit time width of said data signal; when the transition has occurred between two consecutive data in said data signal, said phase comparator circuit outputs a first reference signal, having a time width ranging from the falling edge of said clock signal to the rising edge of said clock signal, and a second reference signal, having a time width ranging from the rising edge of said clock signal to the falling edge of said clock signal,; said charge pump circuit comprises a first charge pump (14) circuit for receiving the input of said first phase error signal and the input of said reference signal, and a second charge pump circuit (24) for receiving the input of said second phase error signal and said second reference signal; and the source current to flow into said loop filter according to the said first and second phase error signals and the sink current to flow into said loop filter (16 and 26) according to said first and second reference signals are designed to become equal with each other when the phase of said data signal and the phase of said clock signal coincide with each other but fails to show the details of the phase comparator or the charge pump. Figure 7 of Summers discloses a phase comparator (701-706 and 710) and a charge pump (203 and 707). It would be obvious at the time the invention was made to one of ordinary skill in the art to use the for the purpose of synchronizing the data pulses.

With respect to claim 8 the above combination produces the CDR circuit as defined

in claim 7, wherein said charge pump circuit includes a current supply means (708) to be controlled by external voltage ((+) or (-)) so as to adjust the ratio between said source current and said sink current.

Allowable Subject Matter

8. Claims 2 and 10 are allowed.

With respect to claim 2, the prior art of record fails to suggest or disclose the phase comparator circuit wherein the output of the second latch is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as a first phase error signal and the output of said first latch circuit is connected to a second delay circuit, an exclusive OR output from the delay circuit and the output from said fourth latch is used as a second phase error signal.

With respect to claim 10, the prior art of record fails to suggest or disclose a CDR circuit including a phase comparator circuit wherein the output of the second latch is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as a first phase error signal; the output of said first latch circuit is connected to a second delay circuit, an exclusive OR output from the delay circuit and the output from said fourth latch is used as a second phase error signal; and said first and second phase error signal are outputted to said charge pump circuit.

Response to Arguments

9. Applicant's arguments filed 7/3/2007 have been fully considered but they are not persuasive.

With respect to applicant's arguments that the operation of the latches differs from the operation of the D type flip-flop, the examiner points out that this is mere allegation because the claimed invention reads on the D-type flip flops of Summers and Holqvist.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the pulse width of the hase error signal Error 1 and the pulse width of the phase error signal Error 2 are to be extended 1.5 times respectively) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With response to applicant's argument that Holmqvist and Summers do not disclose or suggest that the pulse width of the phase error signal is extended by the time width corresponding to the unit time width of the data signal, the Examiner disagrees. The definition of corresponding (according to Merriam-Websters's collegiate dictionary 10th edition) is having or participating in the same relationship, related. Any input is related to the output and therefore the unit time width of the data signal is

related to the pulse width of the phase error signal. The signal is extended by any delay. Because there is an inherent delay in the operation of the circuit the phase error signal is extended by the time width related to the unit time width of the data (input) signal.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation comes from the abstract of Summer using the phase comparator and the charge pump for the purpose of a control voltage to synchronizing the data pulses.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on Mon-Fri (8:30-5:00). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
7/31/2007

Quan Tra
Primary Examiner